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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,833	07/23/2003	Amit Ramchandran	021202-003710US	9239

37490 7590 12/08/2005

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EXAMINER	
SORRELL, ERON J	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,833	RAMCHANDRAN, AMIT	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 2005/0166038 hereinafter "Wang").

3. Referring to claim 1, Wang teaches a data path circuit in a digital processing device (see figure 2), wherein the data path circuit is coupled to a memory bus (see bi-directional busses connected to item 220 in figure 2) for obtaining values from a memory, the data path circuit comprising:

a first plurality of data lines (see bi-directional busses coupling item 216 to 218 in figure 2);

a first data address generator (see item 218 in figure 2)) for coupling the first plurality of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto the first plurality of data lines (see bi-directional busses connecting item 216 to item 218 then item 218 to item 220 in figure 2);

one or more functional units for performing a digital operation coupled to the plurality of data lines (see item 216 in figure 2); and

a register coupled to the first plurality of data lines (see item 214 in figure 2), wherein the register selectively stores a value from the first plurality of data lines so that the value is selectively available on the first plurality of data lines (see paragraph 78 on page 6).

4. Referring to claim 2, Wang teaches the register includes a register file (see item 214 in figure 2) for selectively storing multiple values from the first plurality of data lines and for selectively applying the stored multiple values to the first plurality of data lines (see paragraph 78 on page 6).

5. Referring to claim 3, Wang teaches a control signal coupled to the register for controlling storage of a value from the first plurality of data lines (see paragraph 75 on page 6).

6. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Mirsky (U.S. Pub. No. 2001/0029515).

Referring to claim 10, Mirsky teaches a digital processing system comprising:

a multiplier (see item labeled "multiplier" in figure 4);

an accumulator (see item labeled "accumulator" in figure 4);

a configurable data path coupled to the multiplier and the accumulator (see paragraph 45 bridging pages 2 and 3); and

a direct data path coupled between the multiplier and the accumulator (see buses and registers coupled between the multiplier and accumulator).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4,8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Mirsky (U.S. Pub. No. 2001/0029515).

9. Referring to claim 4, Wang teaches the datapath circuit of claim 1, however Wang fails to teach a data field is used to select loading of a value on the memory bus of selectable bit width.

Mirsky teaches, in an analogous system, the above limitation (see paragraph 69 on page 5).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Wang with the teachings of Mirsky. One of ordinary skill in the art would have been motivated to make such modification in order to dynamically configure the system in accordance with the processing demands as suggested by Mirksy (see paragraph 44 on page 2).

10. Referring to claims 8 and 9, Wang teaches the datapath circuit of claim 1, however, Wang fails to teach the functional units include a multiplier and accumulator, the data path circuit further comprising a coupling of the multiplier to the plurality of data path lines; a coupling of the accumulator to the plurality of data path lines; direct data lines coupled between the multiplier and the accumulator, wherein the direct data lines are uni-directional for transferring data from the multiplier to the accumulator.

Mirsky teaches, in an analogous system, the above limitations (see figure 4 and paragraph 52 on page 3).

11. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Wang with the above teachings of Mirsky. One of ordinary skill in the art would have been motivated to make such modification to be able to perform complex digital signal processing functions.

12. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Abbott et al. (U.S. Patent No. 6,601,158 hereinafter "Abbott").

13. Referring to claim 5, Wang teaches the datapath circuit of claim 1, however, Wang teaches the system further comprises a second plurality of data lines (see figure 2), however Wang fails to teach a second data address generator for coupling the second plurality of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto the second plurality of data lines; and wherein the second data address generator is responsive to a control signal for selectively providing a data value from the first plurality of data lines to the second plurality of data lines.

Abbott teaches, in an analogous system, the above limitations (see lines 12-45 of column 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Wang with the above teachings of Abbott. One of ordinary skill in the art would have been motivated to make such modification because Abbott suggests using a plurality of address generators allows the system to process data using complex algorithms such as those using nested loops (see lines 57-67 of column 9).

14. Referring to claim 6, Wang teaches a data path circuit in a digital processing device, wherein the data path circuit is

coupled to a memory bus for obtaining values from a memory, the data path circuit comprising:

a plurality of groups of data lines (see buses in figure 2);

one or more functional units for performing a digital operation coupled to the plurality of groups of data lines (see item labeled 216 in figure 2); and

a plurality of registers coupled to each group of data lines on a one-to-one correspondence, wherein the plurality of registers selectively store values from the plurality of groups of data lines so that the values are selectively available on the plurality of groups of data lines (see item labeled 214 in figure 2).

Wang fails to teach the system comprises a plurality of data address generators for coupling the plurality of groups of data lines to the memory bus so that a value from the memory transferred by the memory bus can be placed onto a group of data lines.

Abbott teaches, in an analogous system, the above limitations (see lines 12-45 of column 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Wang with the above teachings of Abbott. One of

ordinary skill in the art would have been motivated to make such modification because Abbott suggests using a plurality of address generators allows the system to process data using complex algorithms such as those using nested loops (see lines 57-67 of column 9).

15. Referring to claim 7, Wang teaches 8 groups of 16 data lines are used, wherein each group of data lines is coupled to a register file capable of storing 8 16-bit words, wherein each of the data address generators can selectively provide a value on a first group of data lines to a second group of data lines (see item 214 in figure 2 and the associated buses connected thereto).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following U.S. Patent has been cited to further show the state of the art as it pertains to adaptable datapaths:

U.S. Patent No. 6,883,084 to Donohoe teaches a reconfigurable data path for a processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J.

Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
November 29, 2005

KIM HUYNH
PRIMARY EXAMINER

12/05/05